

Networks-on-Chip,

a communication subsystem for next generation VLSI design

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2nd Annual Workshop on Embedded Systems

Outlines

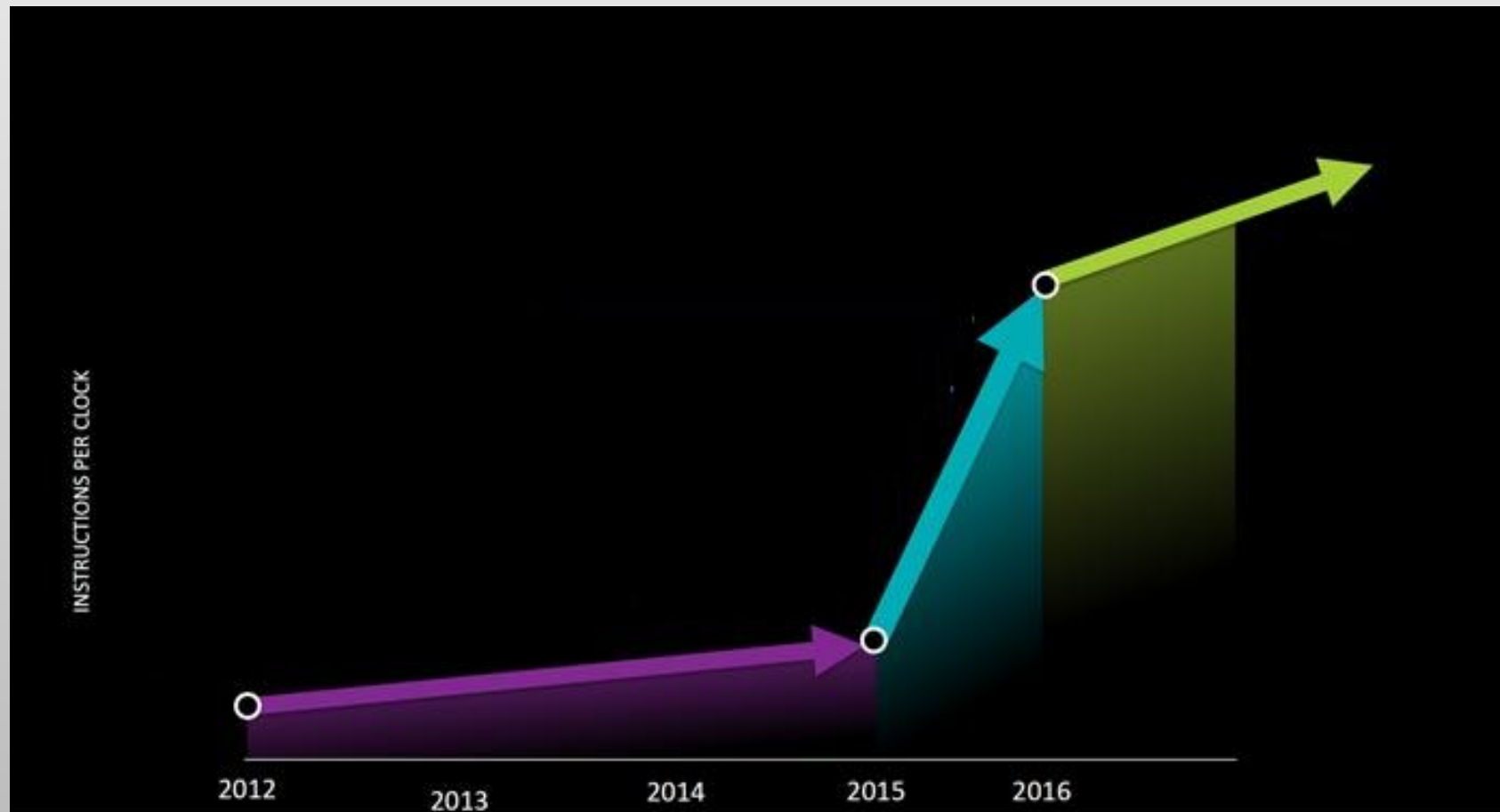
- ▶ Introduction
- ▶ NoC Design Considerations
- ▶ NoC Prototype Examples
- ▶ Research Project 1: Newcastle University
- ▶ Research Project 2: University of York

Introduction



VLSI Trends

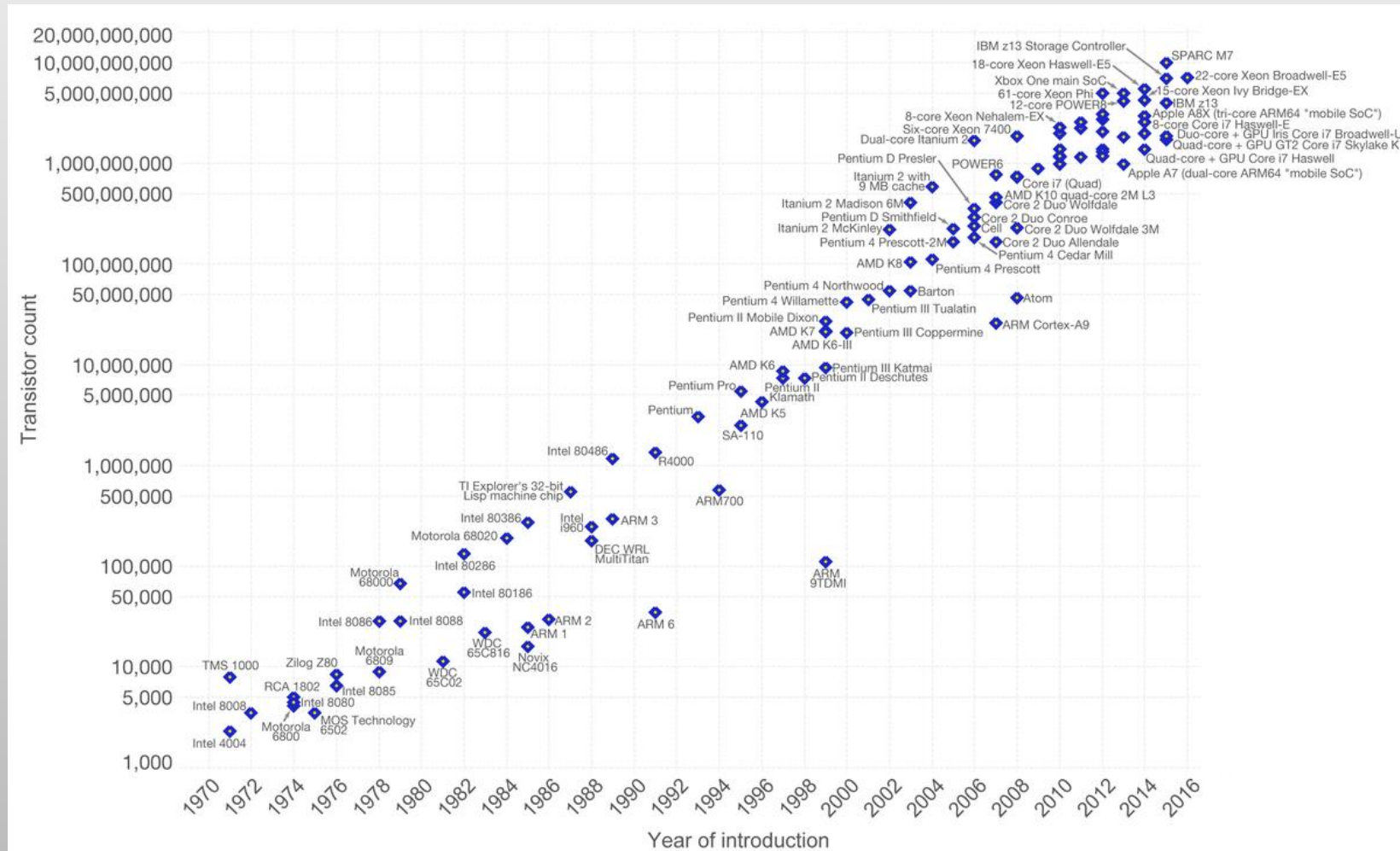
- ▶ Computing industry is performance hungry !



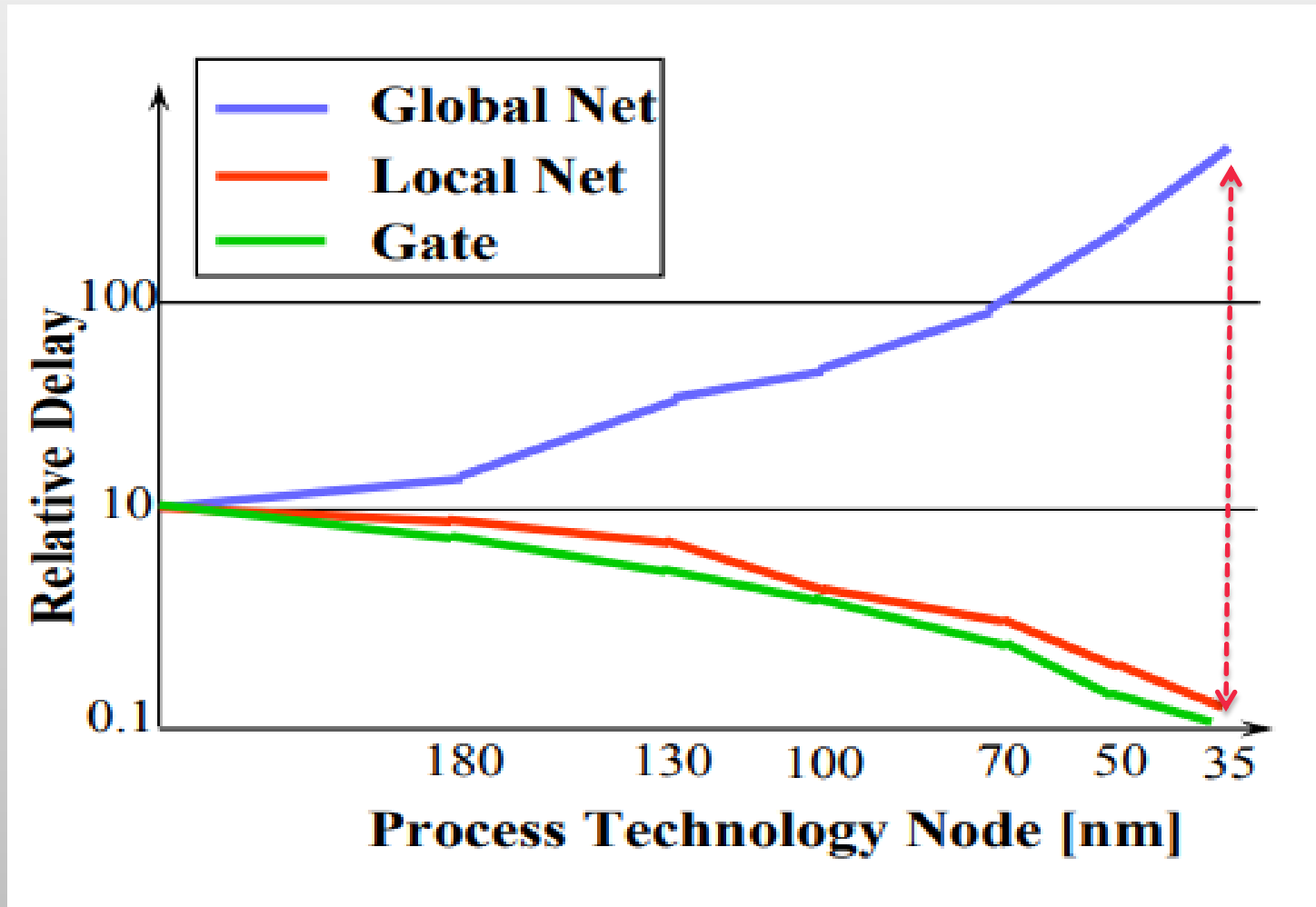
VLSI Trends

- ▶ Technology trends
- ▶ Smaller transistors -> Higher integration density
 - ▶ *Complexity, power and thermal hazards*

Moor's Law



The wire delay Gap

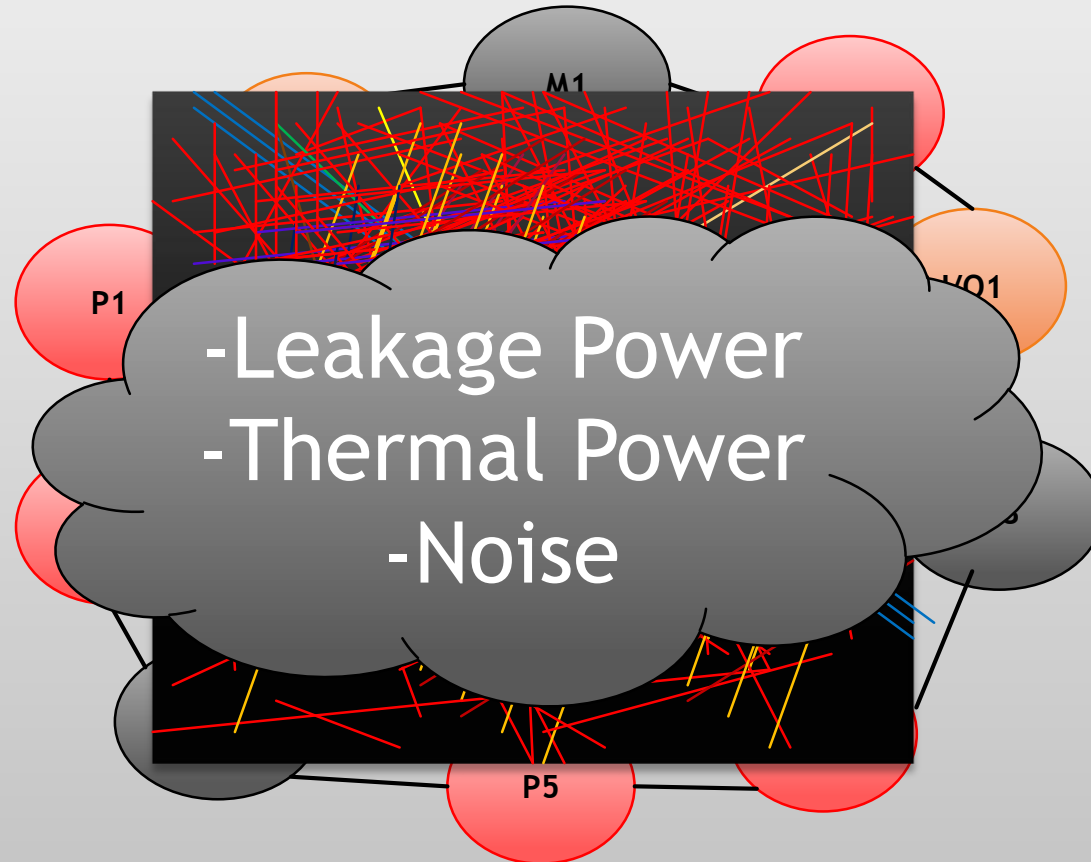


Source: International Technology Roadmap for Semiconductors
(<http://www.itrs2.net/>)

Technology & Architecture Trends

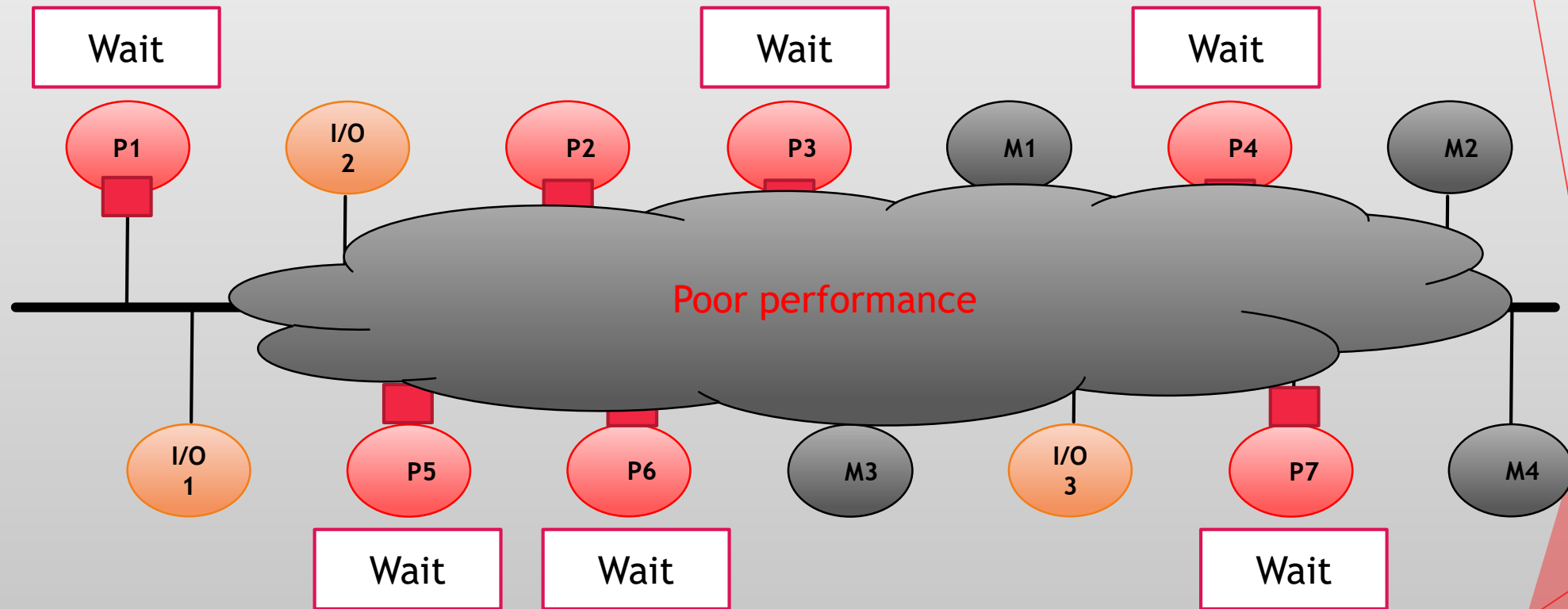
- ▶ Architectural trends
 - ▶ Go parallel!
 - ▶ *Requires: Efficient on-chip communication*
 - ▶ *Key challenges:*
 - ▶ *Scalability*
 - ▶ *Performance*
 - ▶ *Power*

On-chip Interconnection Solutions



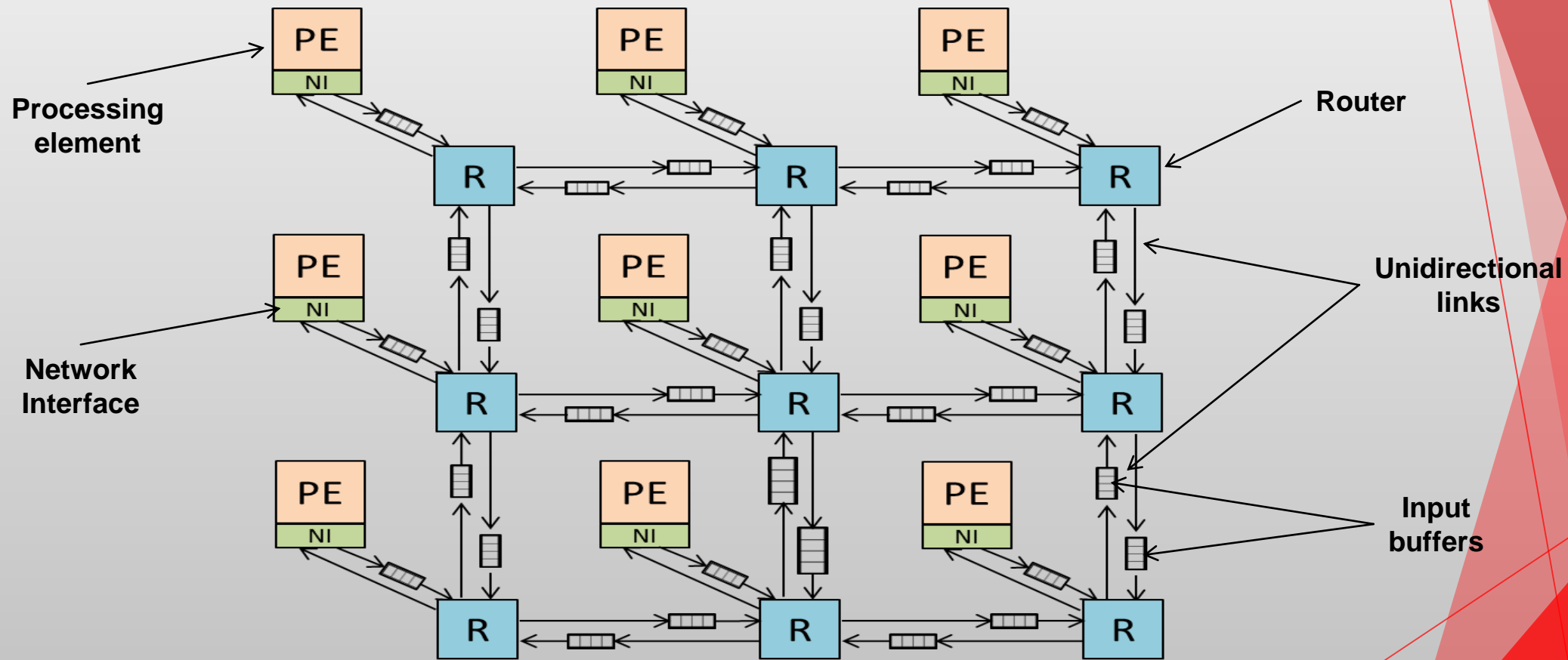
Point-to-Point

On-chip Interconnection Solutions



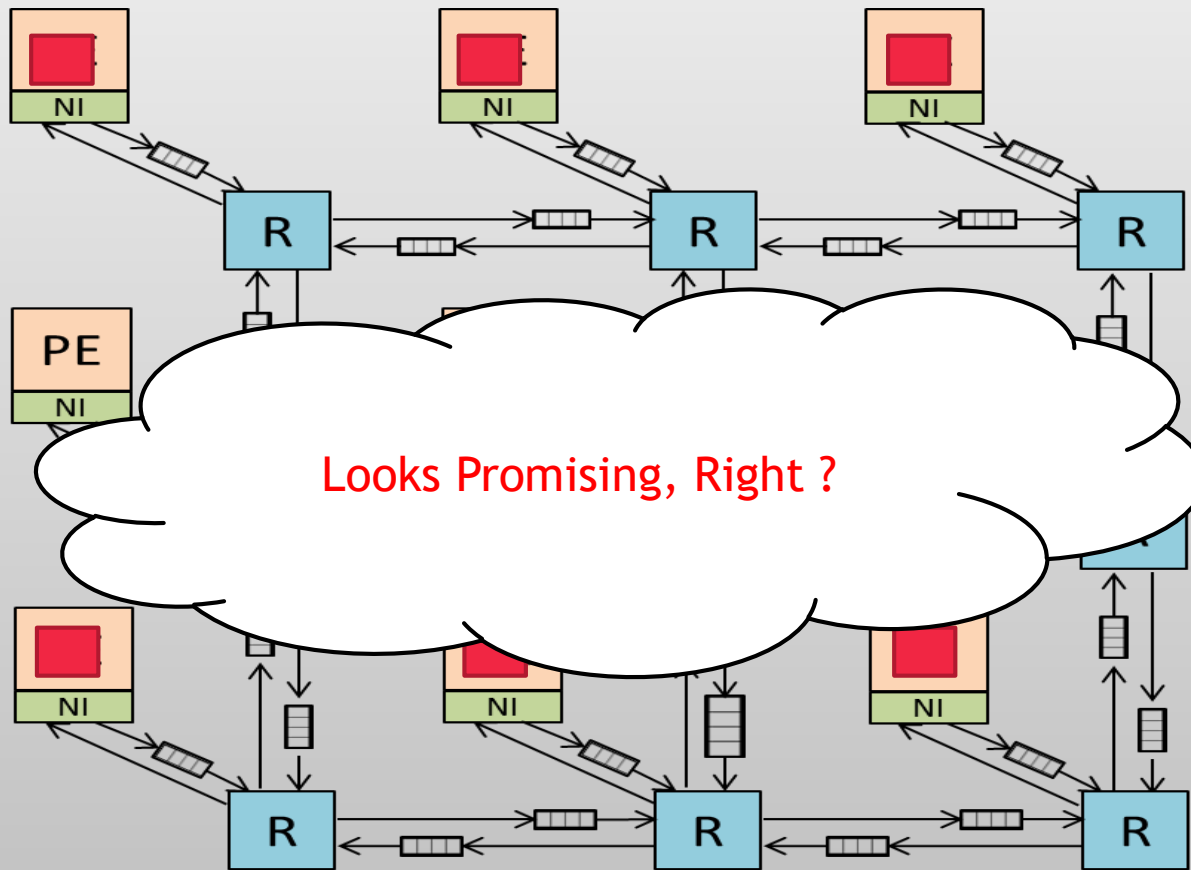
Shared bus

On-chip Interconnection Solutions



Packet Switched Network

On-chip Interconnection Types



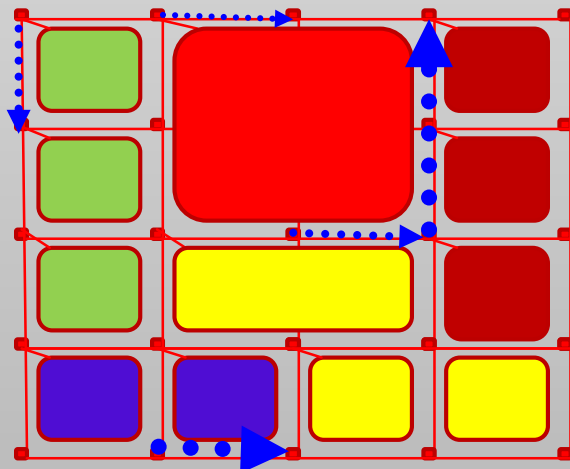
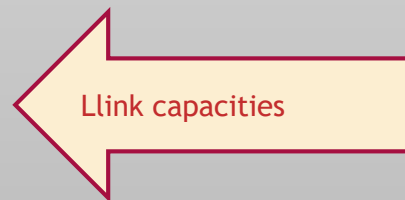
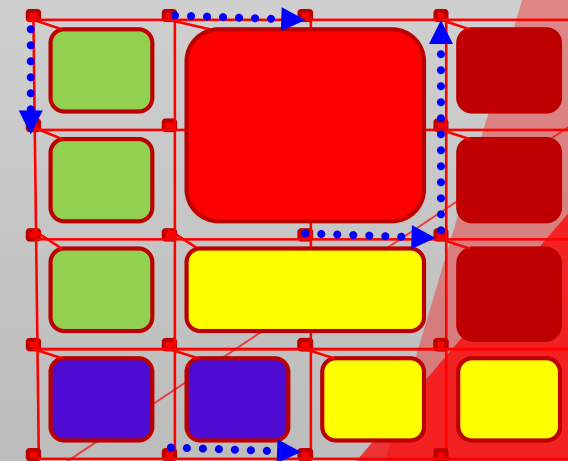
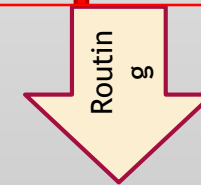
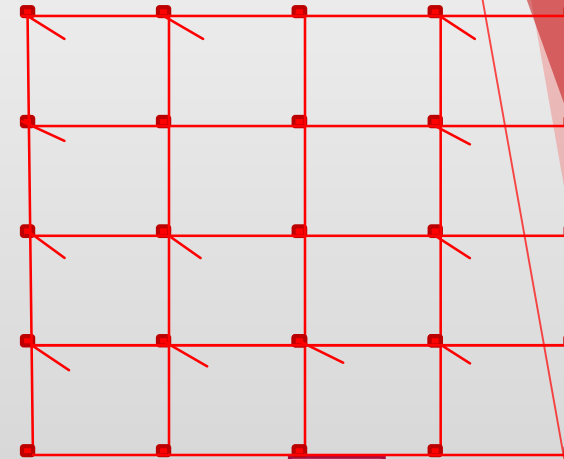
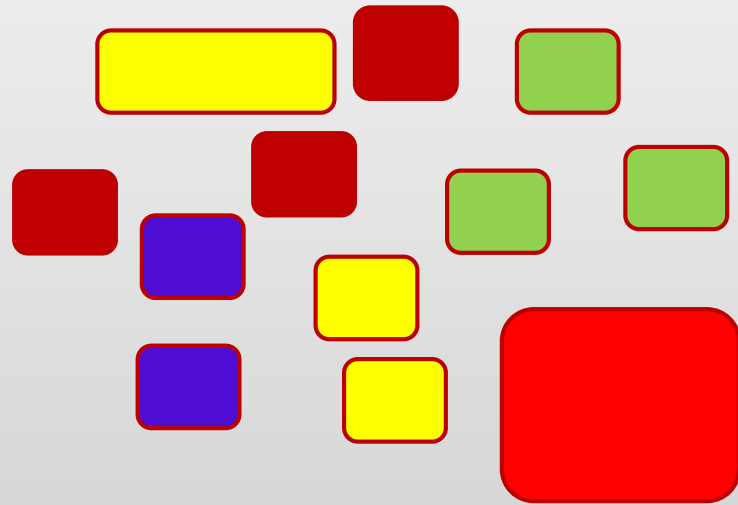
Why NoCs ?

- ▶ Reusability
- ▶ Flexibility and Fault Tolerance
- ▶ Globally Asynchronous Locally Synchronous (GALS)
- ▶ Low Power and Dark Silicon
- ▶ Scalability
- ▶ Standard Design Methods using Layered design framework:
 - ▶ Physical (Links)
 - ▶ Network (Routing)
 - ▶ Application (mapping, scheduling etc.)

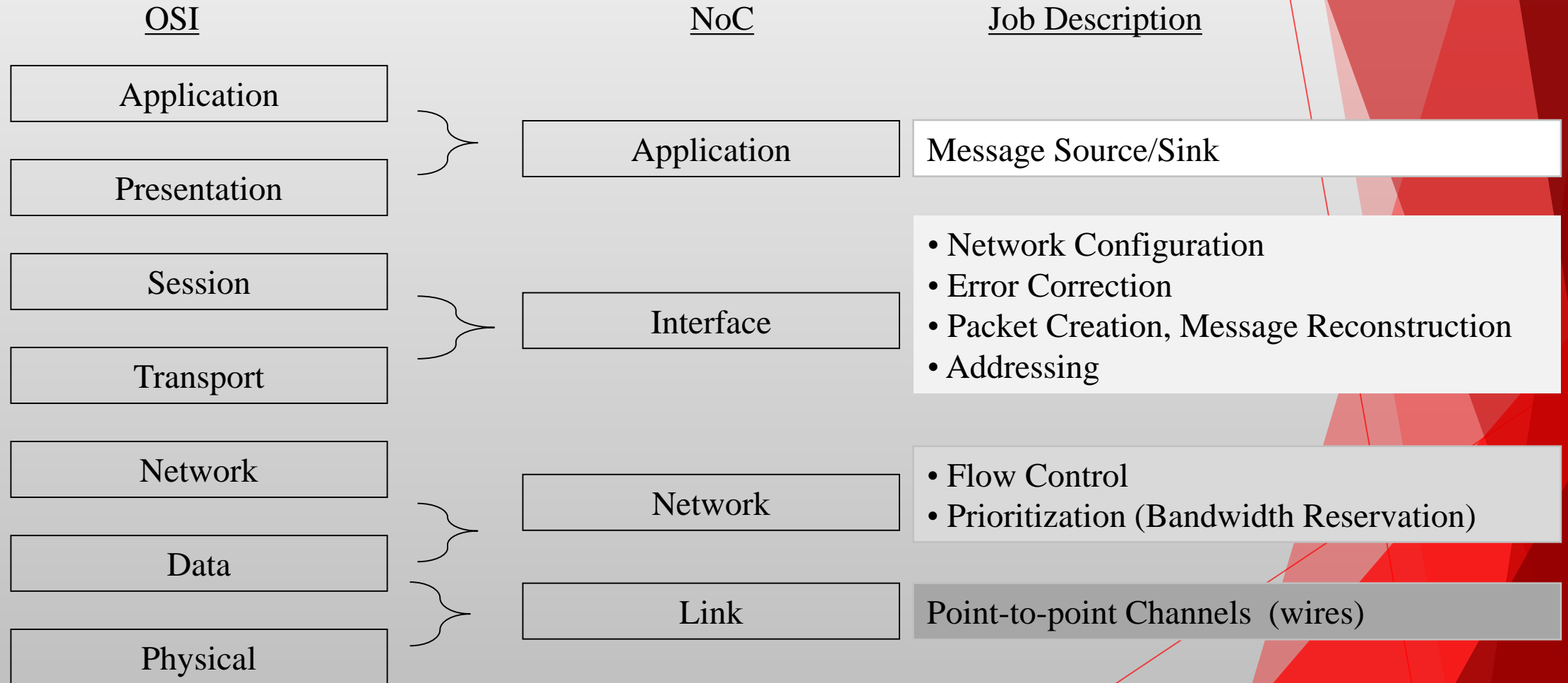
NoC Design Considerations



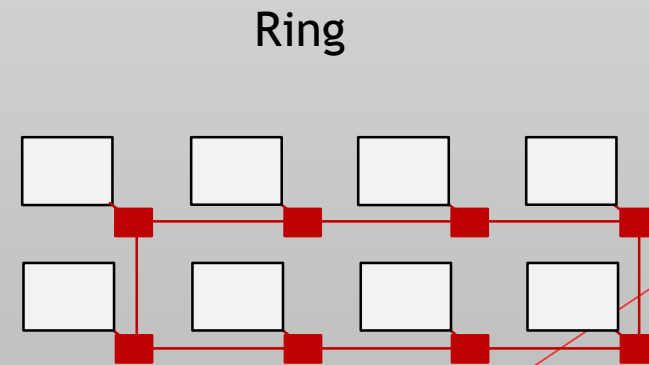
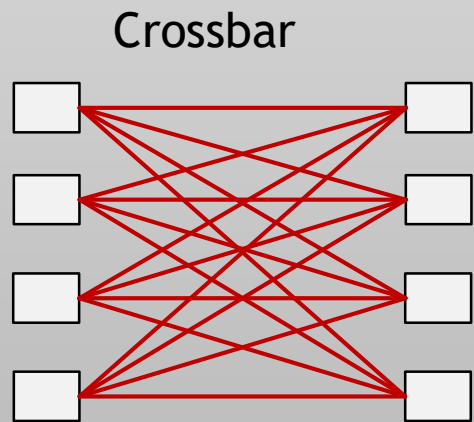
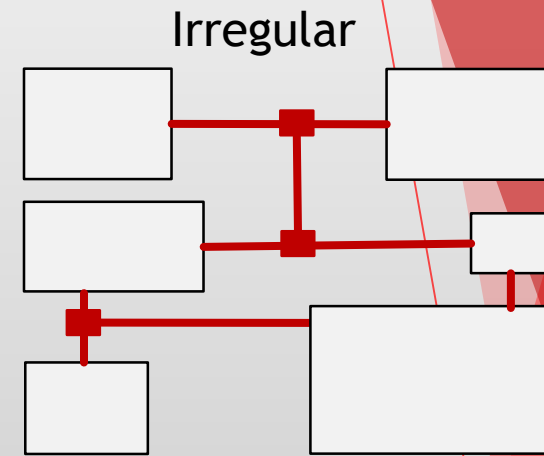
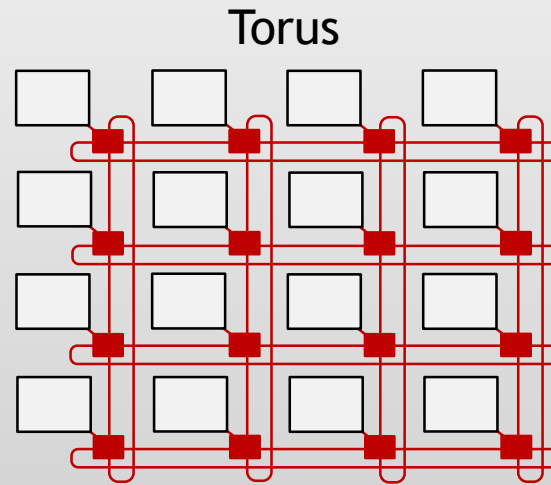
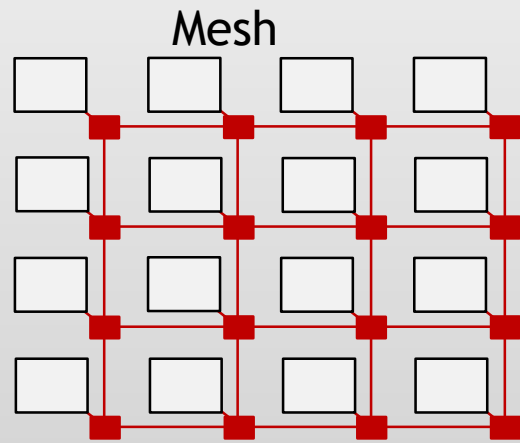
Typical NoC Design Flow



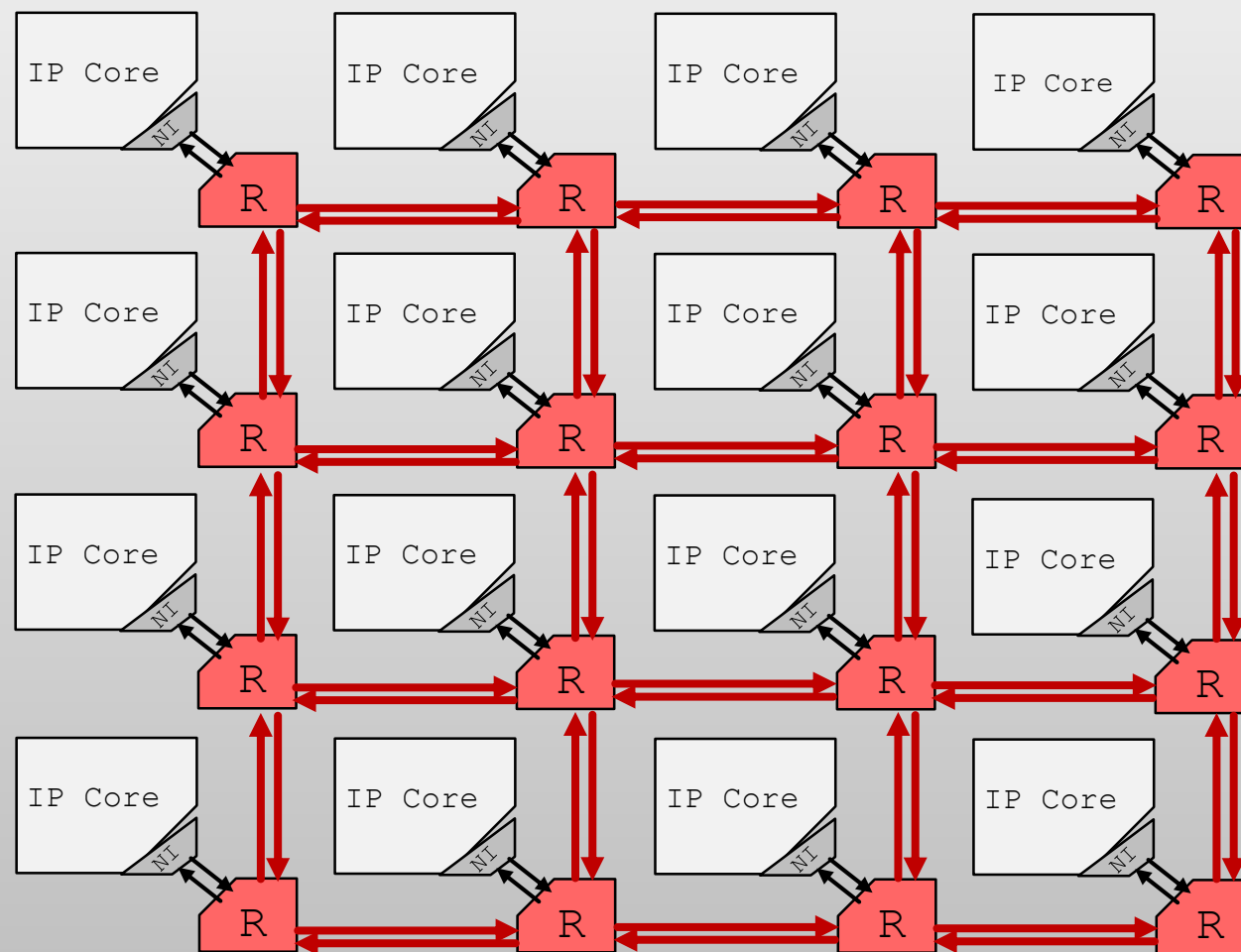
NoC Abstraction vs. OSI



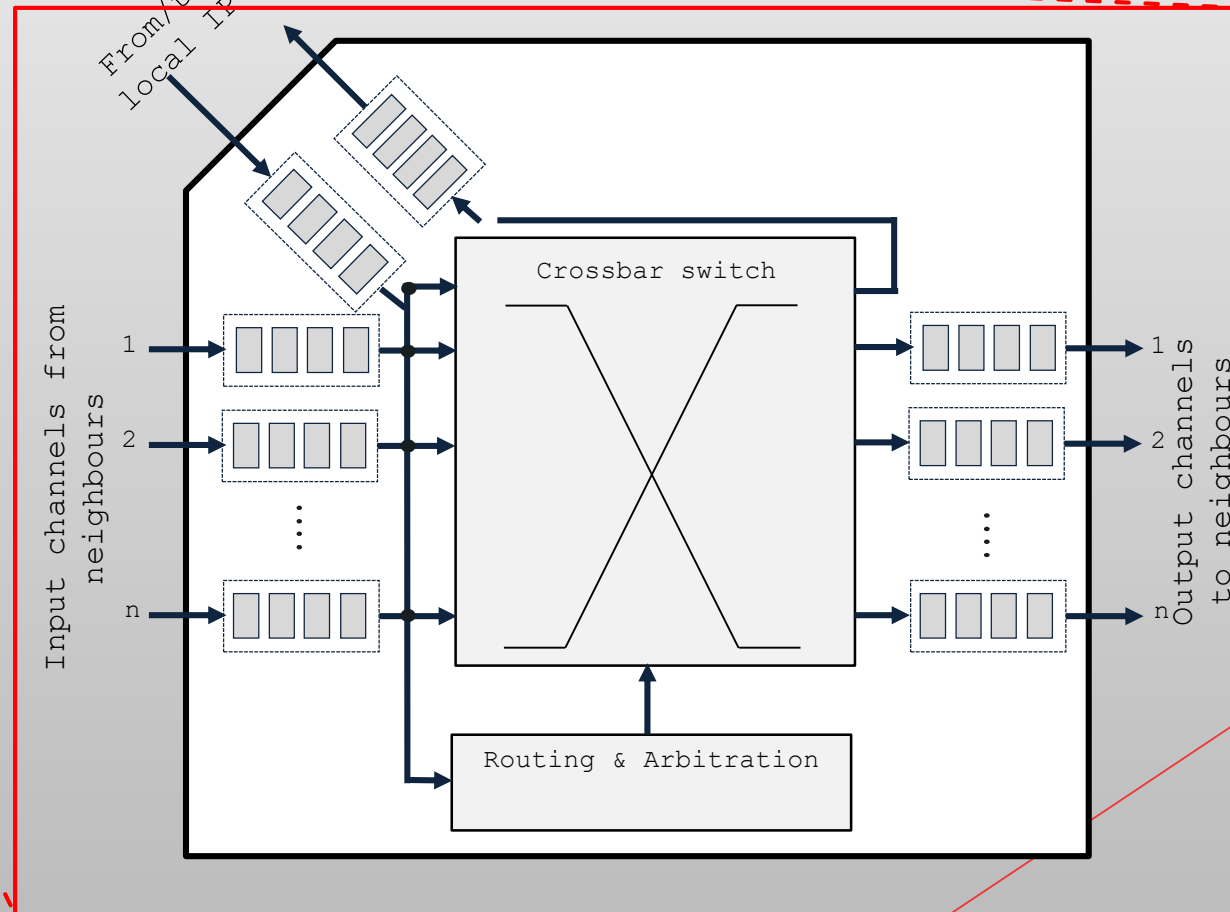
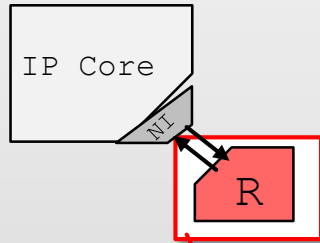
NoC Topologies



Regular Mesh



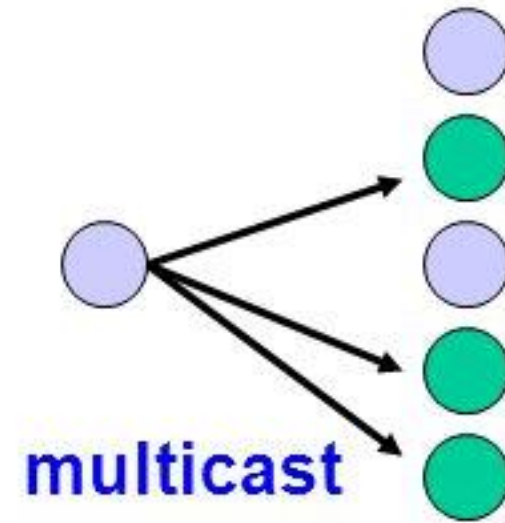
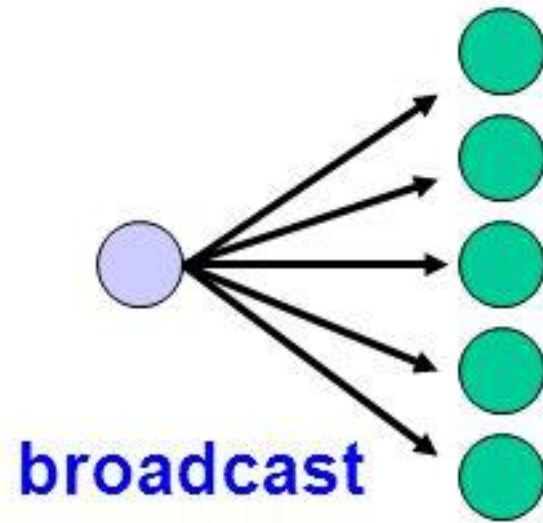
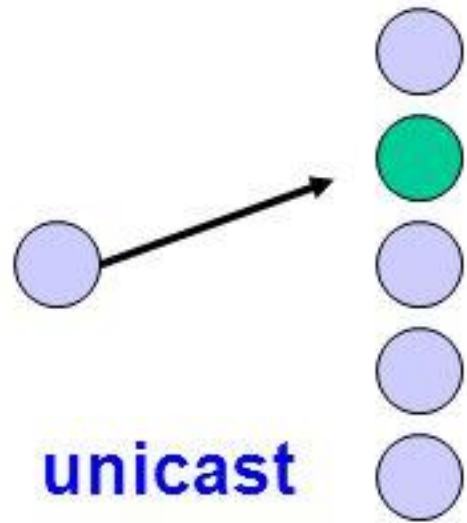
Router Architecture



Routing Algorithm

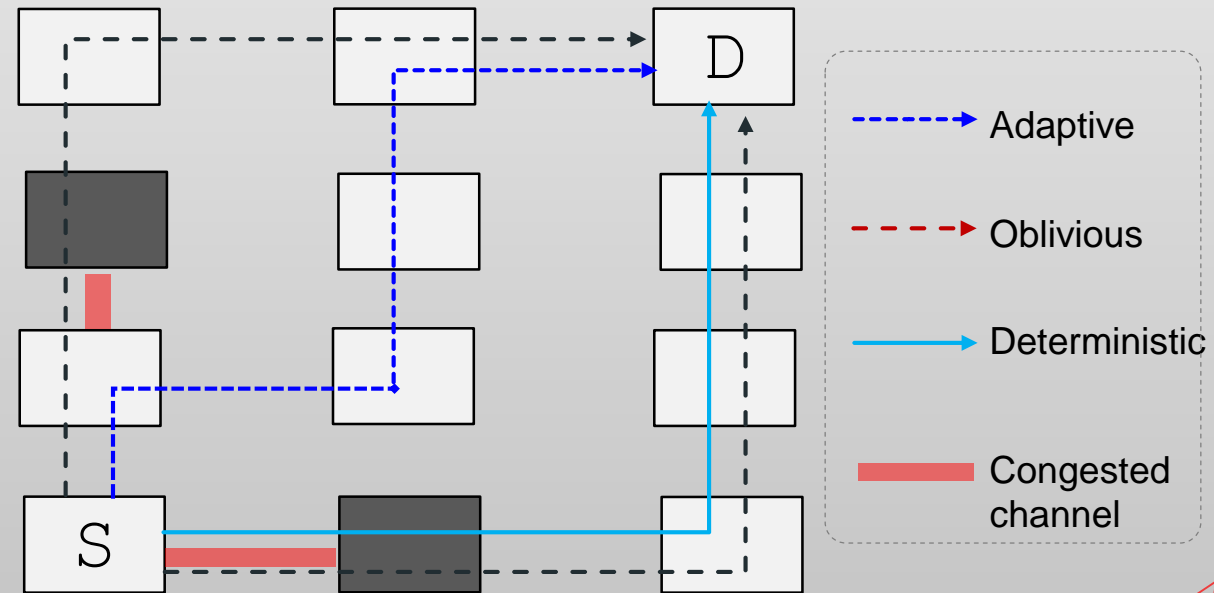
- ▶ Attributed by
 - ▶ Number of destinations
 - ▶ Unicast, Multicast, Broadcast?
 - ▶ Adaptivity
 - ▶ Deterministic, Oblivious or Adaptive
 - ▶ Implementation (Mechanisms)
 - ▶ Source or node routing?
 - ▶ Table or circuit?

Number of destinations



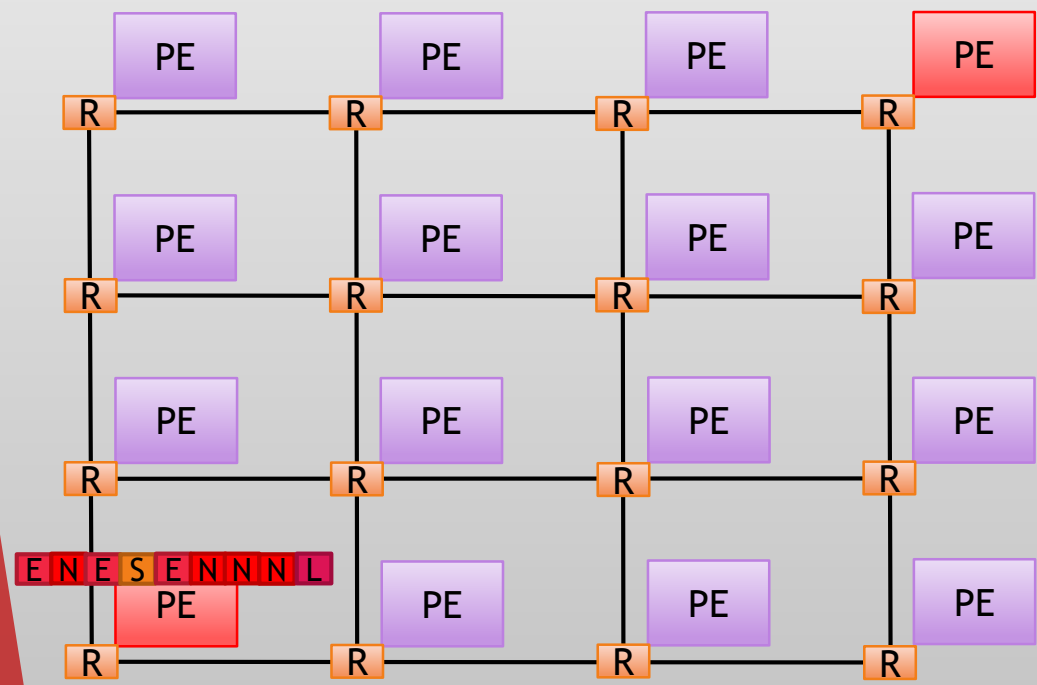
Adaptivity

- ▶ Deterministic or static
- ▶ Adaptive
- ▶ Oblivious

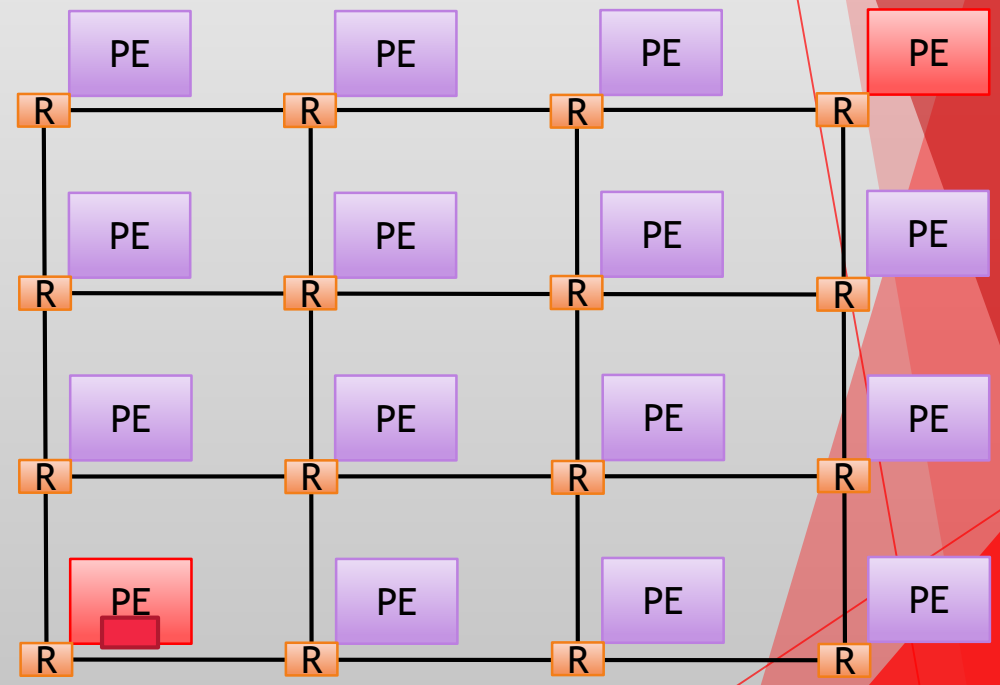


Implementation (Mechanisms)

Source Routing

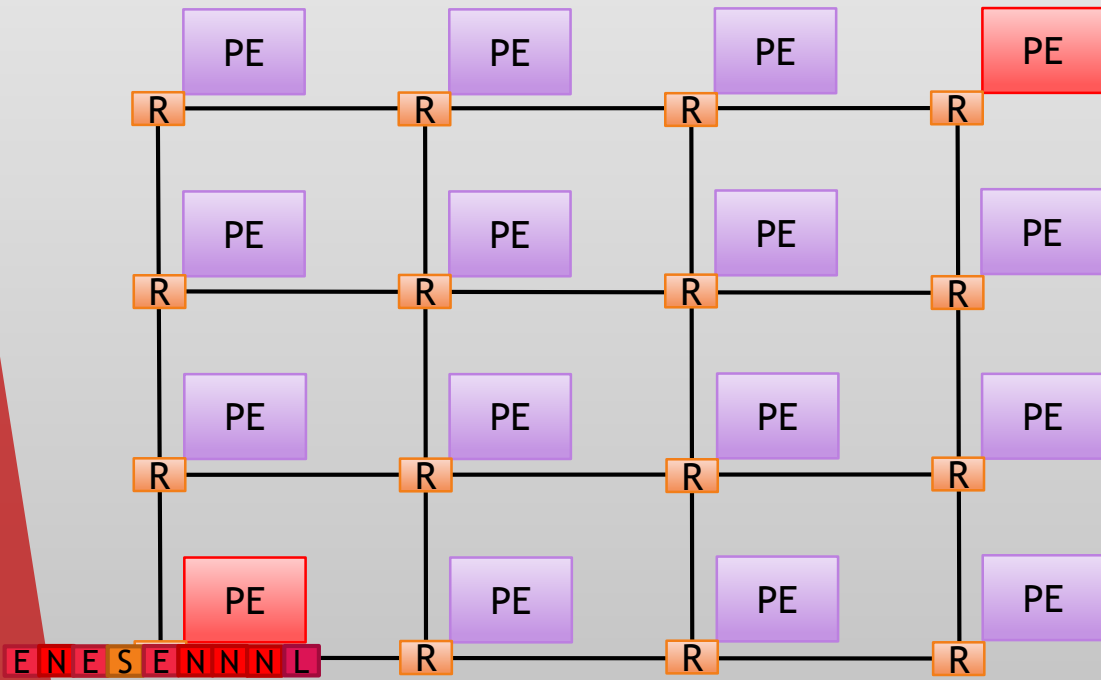


Distributed Routing

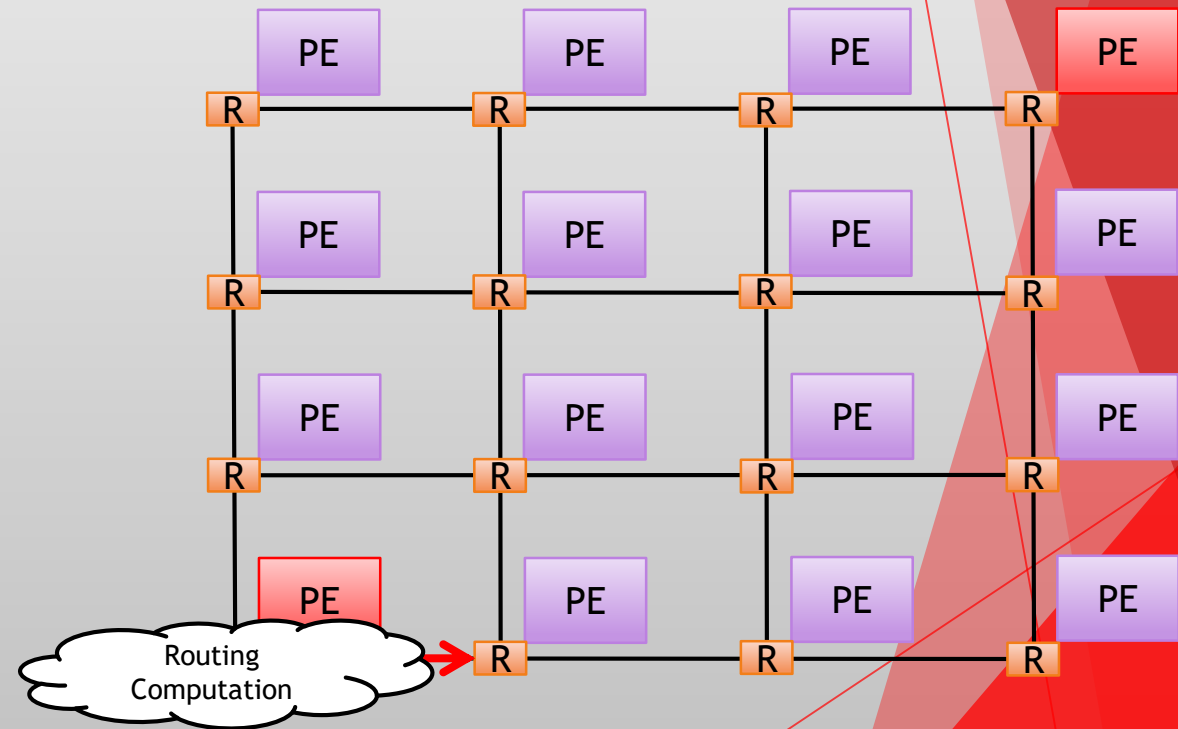


Implementation (Mechanisms)

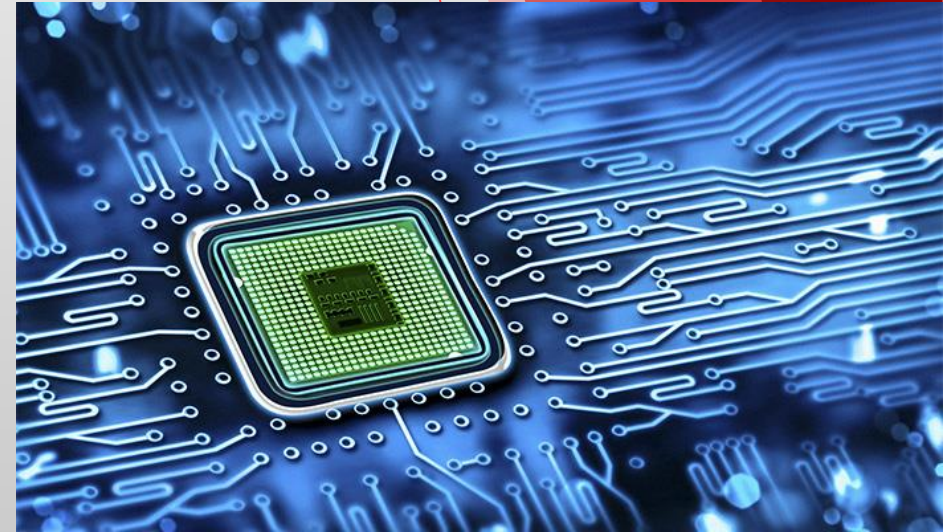
Source Routing



Distributed Routing

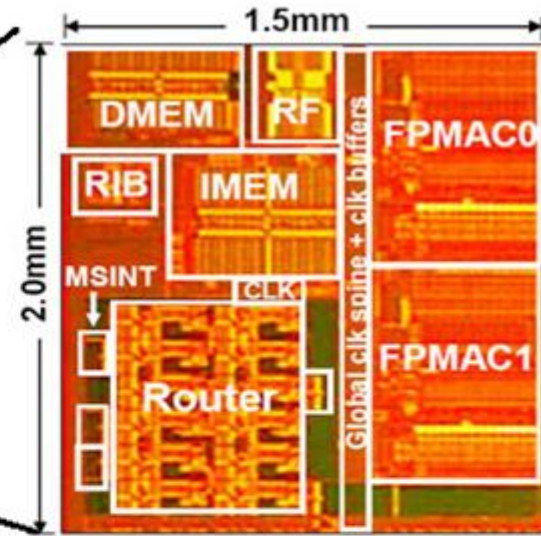
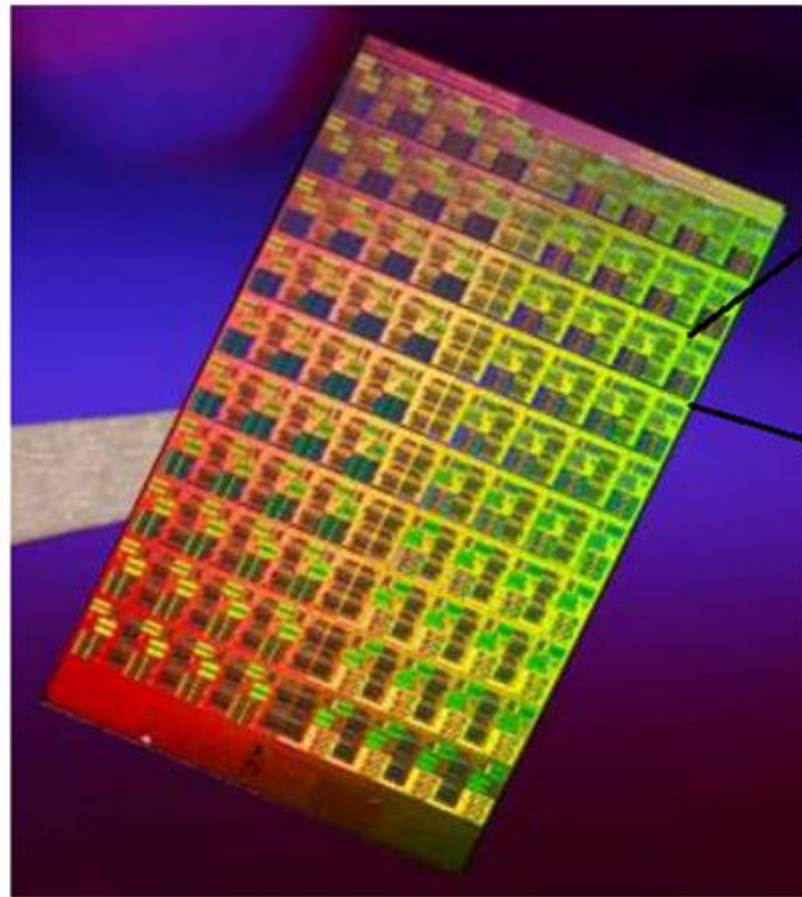


NoC Prototype Examples



NoC Prototype Examples

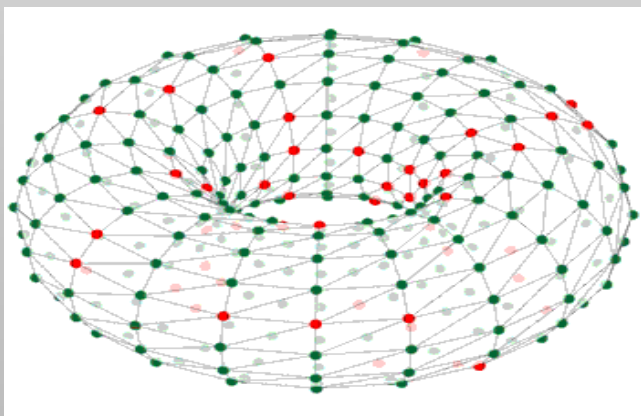
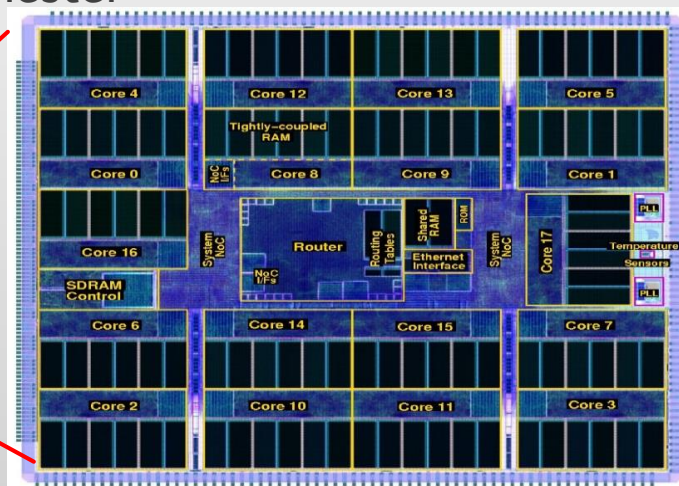
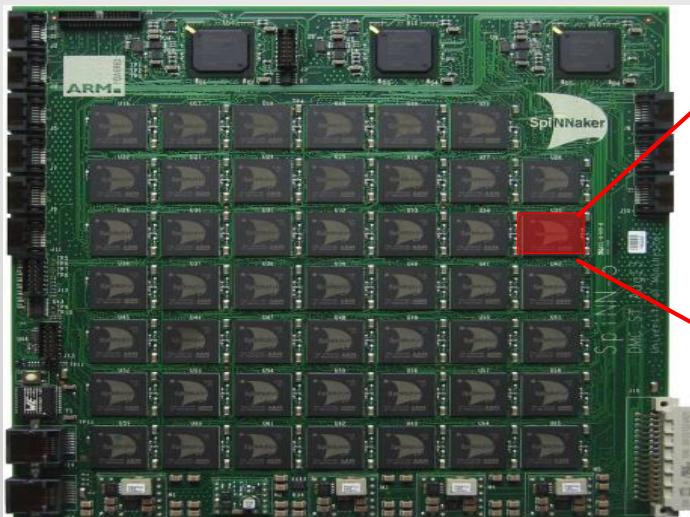
- ▶ Intel's Teraflops (80 core research chip)



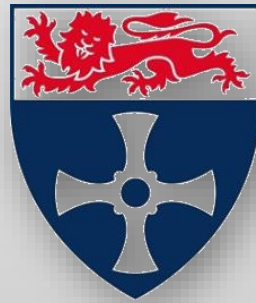
Technology	65nm CMOS Process
Interconnect	1 poly, 8 metal (Cu)
Transistors	100 Million
Die Area	275mm ²
Tile area	3mm ²
Package	1248 pin LGA, 14 layers 343 signal pins

NoC Prototype Examples

- ▶ SpinNaker System, University of Manchester

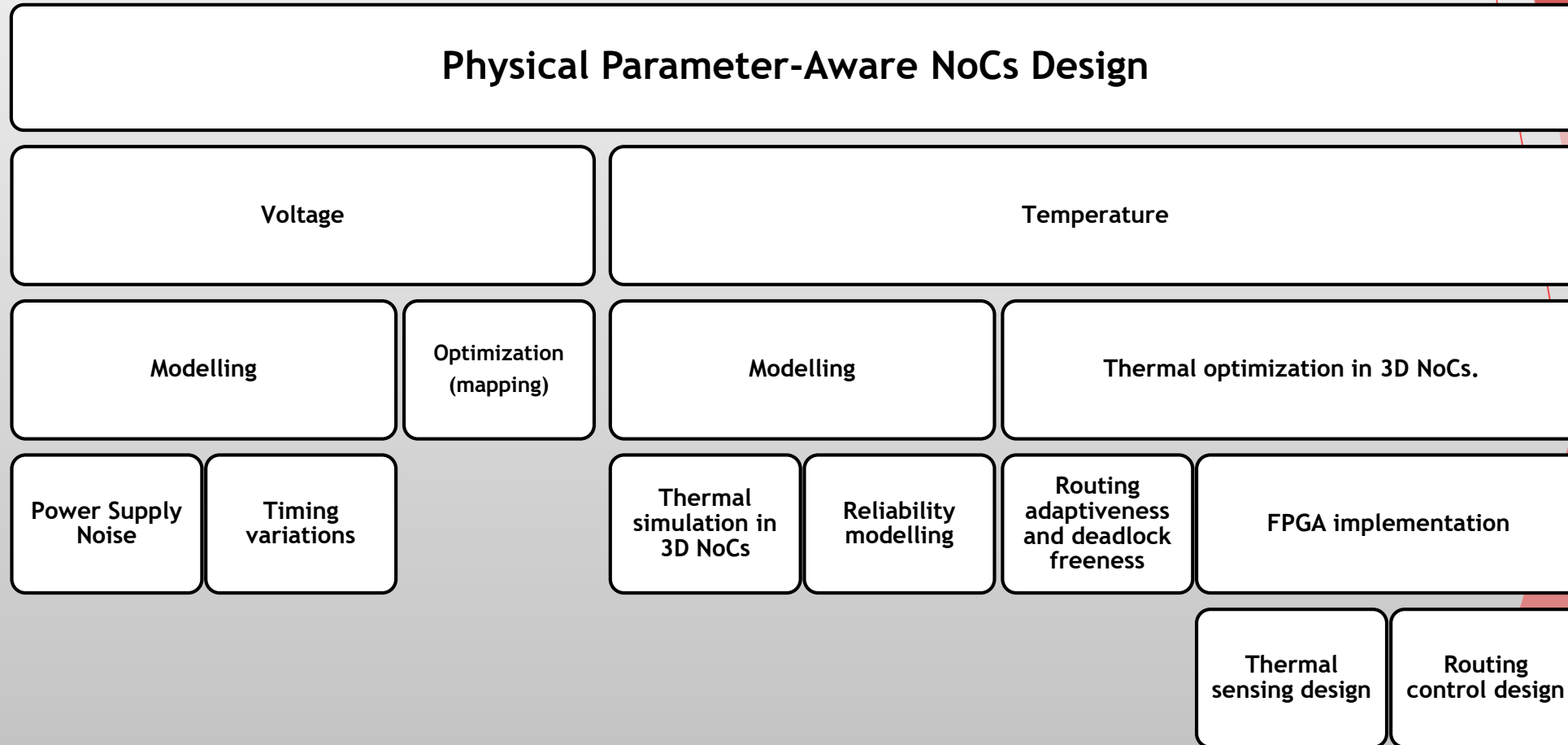


Research Project 1



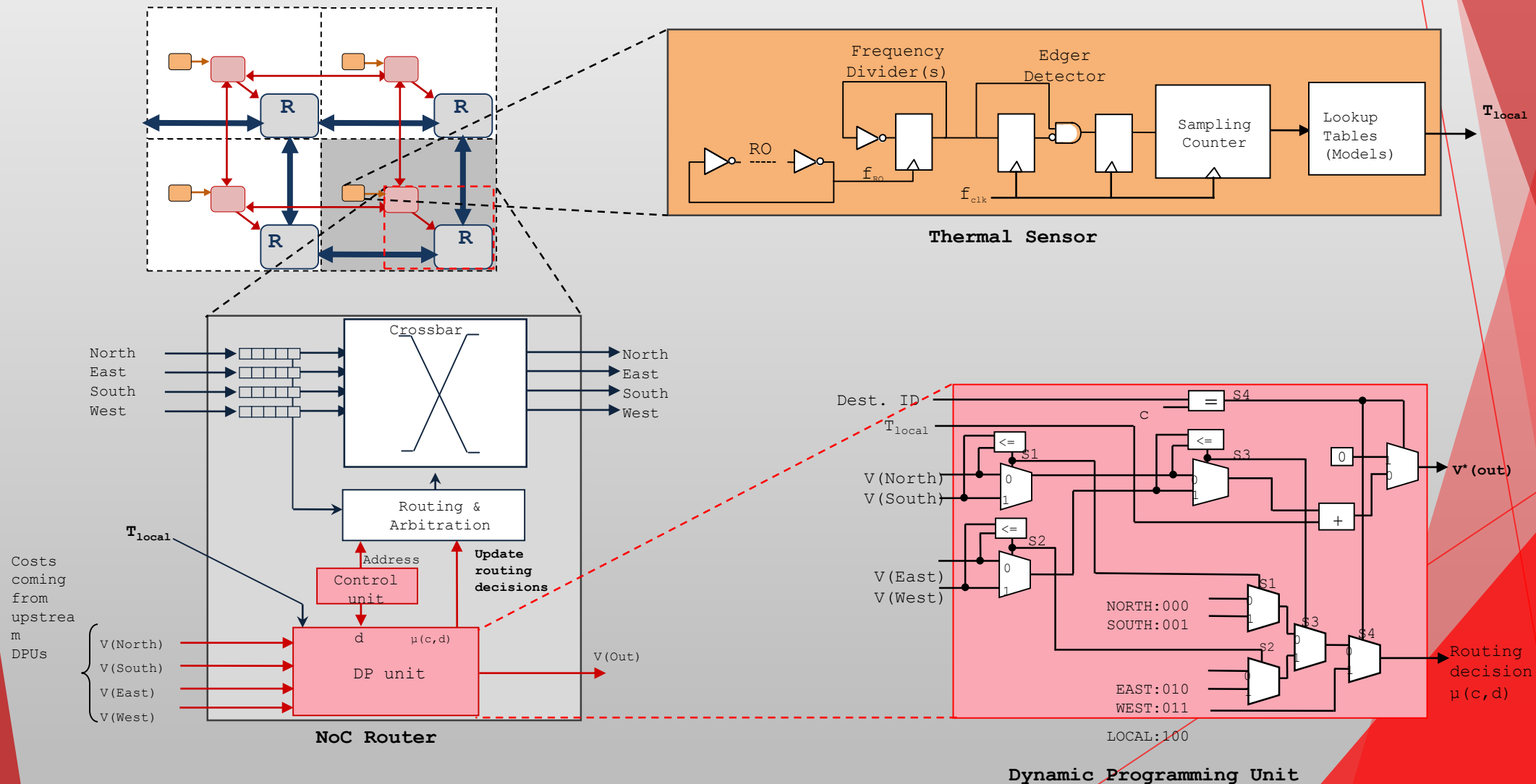
Newcastle
University

Research Project 1: Newcastle University



Research Project 1: Newcastle University

FPGA Implementation of Thermal-Adaptive Routing

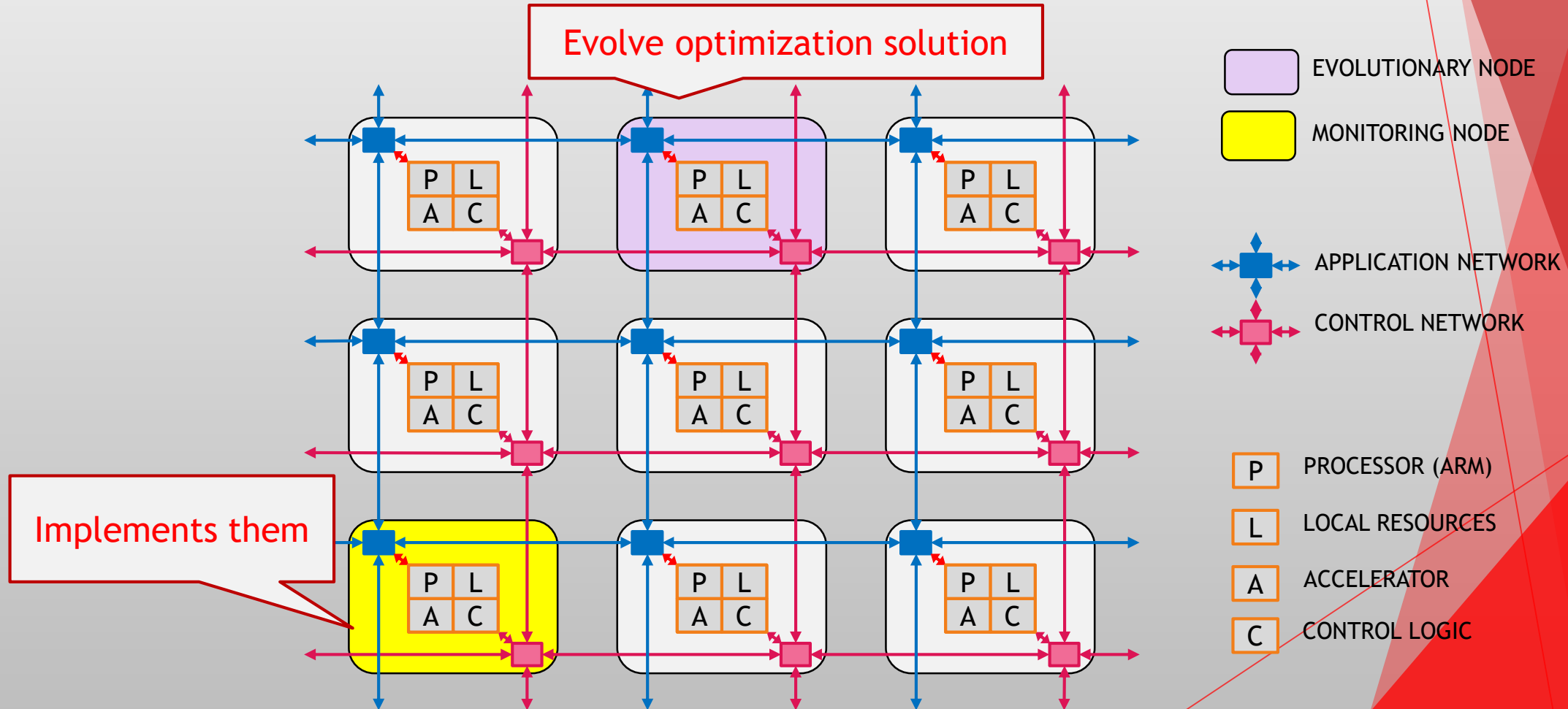


Research Project 2



Research Project 2: University of York

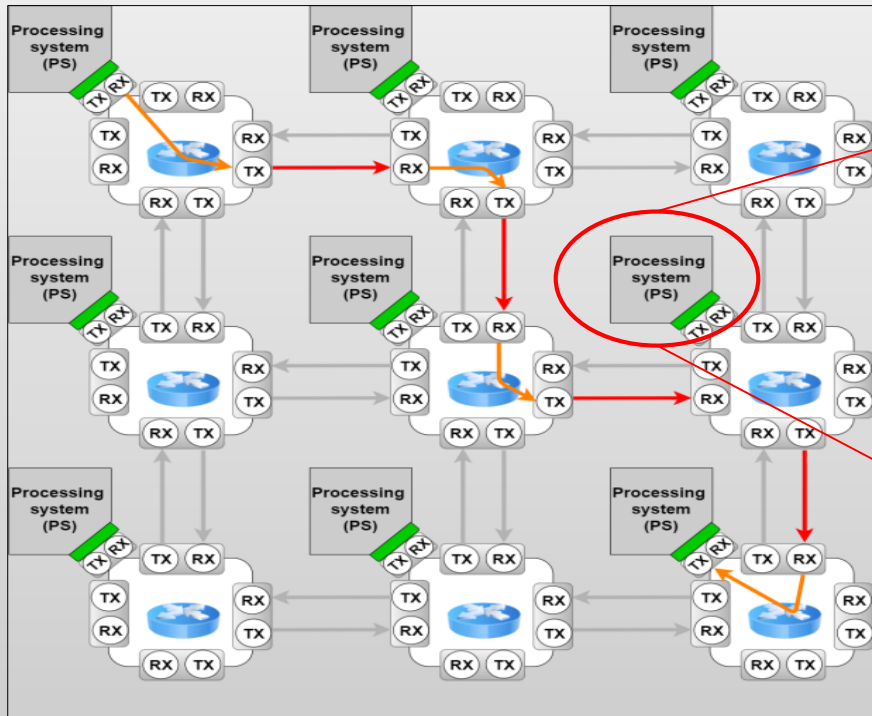
- ▶ Continuous on-line adaptation in many-core systems



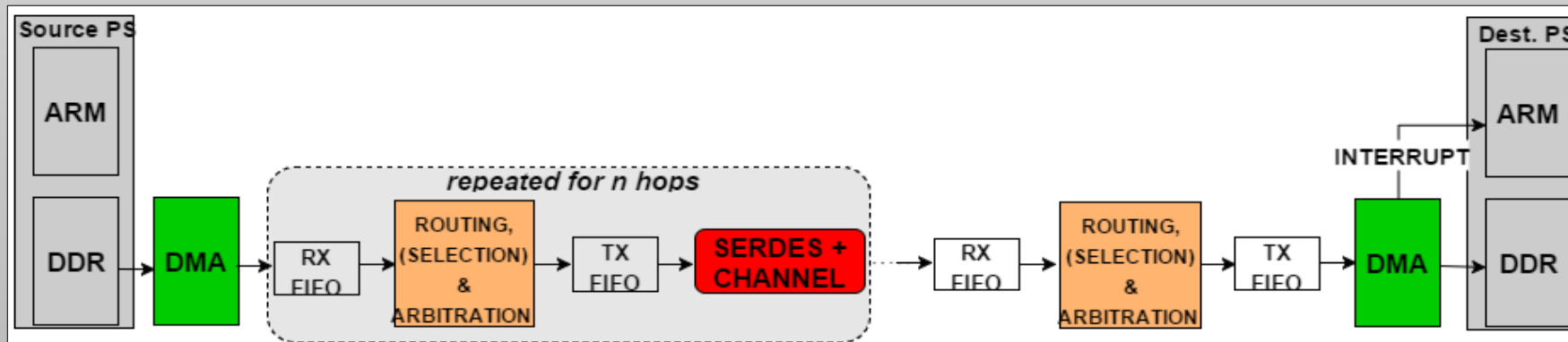
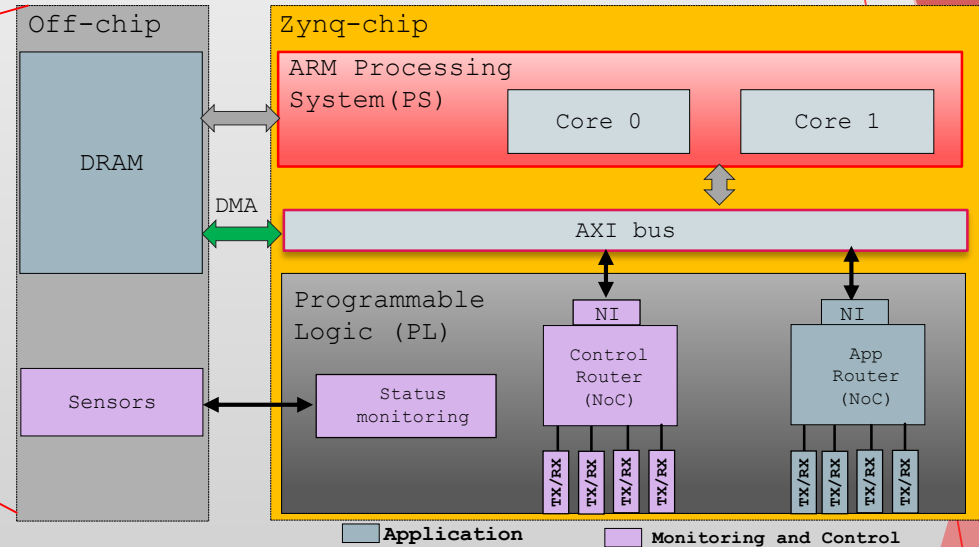
Research Project 2: University of York

- Continuous on-line adaptation in many-core systems
 - ❑ **Monitoring**
 - ❑ Power, Temperature, Quality-of-Service (QoS), Faults
 - ❑ **Control**
 - ❑ Frequency, Voltage, Application mapping, NoC Routing
 - ❑ **Optimisation**
 - ❑ Evolutionary Algorithms (e.g GA, ACO etc.)
 - ❑ **Aims at**
 - ❑ Reliability
 - ❑ Performance
 - ❑ Scalability

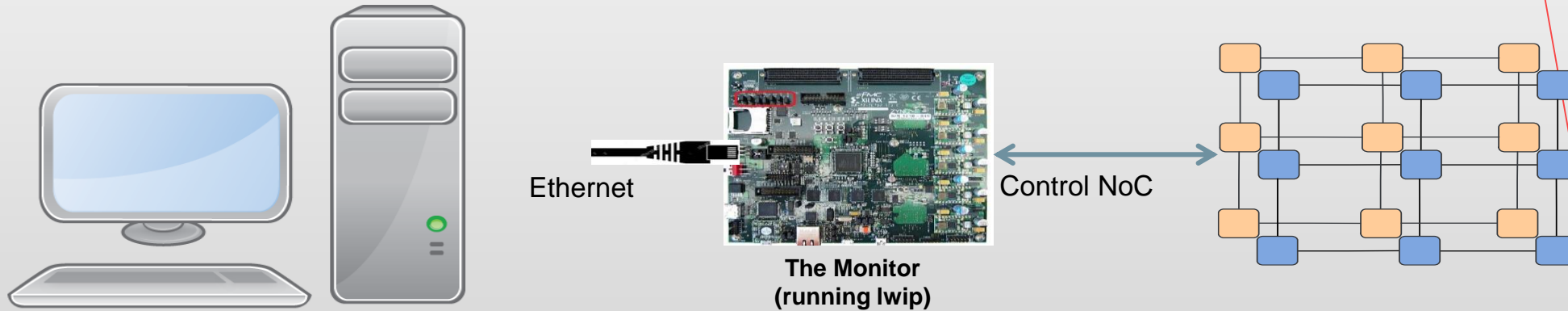
Research Project 2: University of York



Xilinx ZC 7020 FPGA Board



Research Project 2: University of York

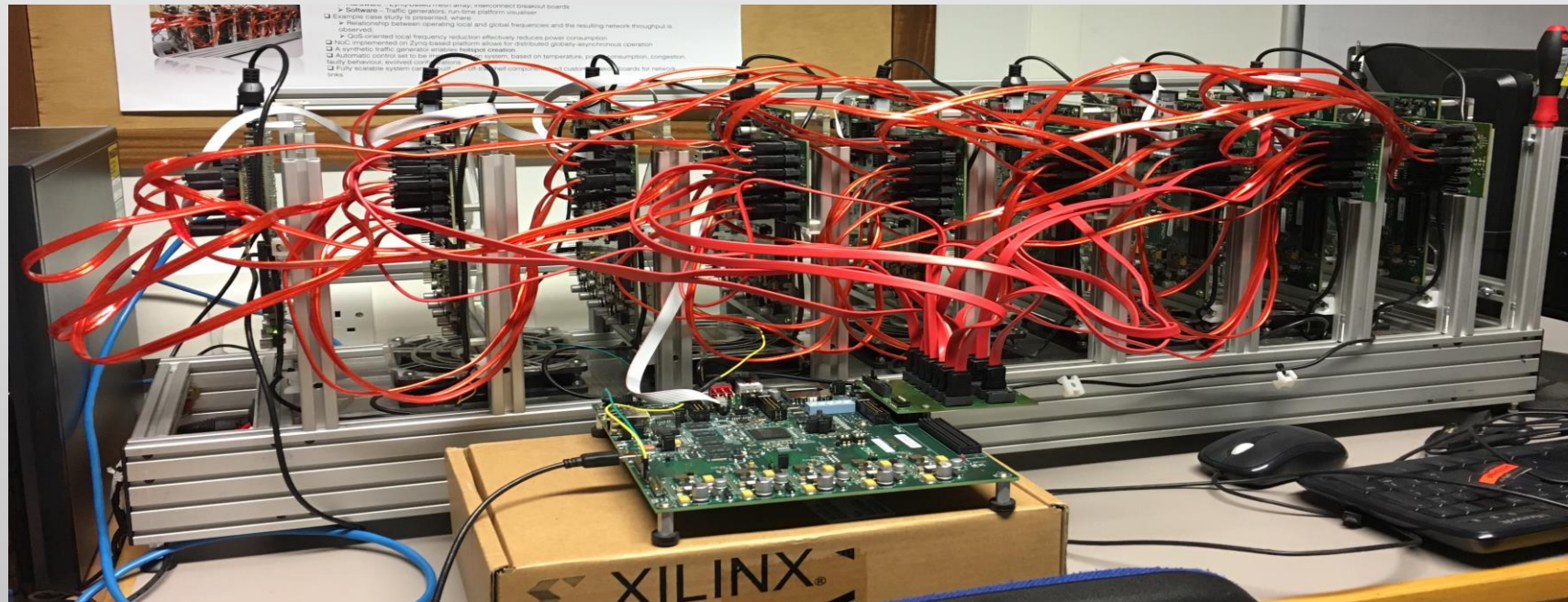


```
nd706@228: ~/work/graceful/graceful-v9s
nd706@228:~/w... x nd706@228:~/w... x nd706@228:~/w... x nd706@228:~/w... x
nd706@228:~/work/graceful/graceful-v9s$ telnet 192.168.1.10 7
Trying 192.168.1.10...
Connected to 192.168.1.10.
Escape character is '^]'.
h
-----
Graceful Monitoring Node
-----
a: send status
o: set observation channel
c:clear data rx buffer
d: display status
e: traffic element [en/disable]
f: set frequency
g: check node
h: help
i: set node id
j: dump observation buffer
k: sink data
l: set fctrl beta
m: set routing mode
n: enable frequency control
b: set observation node
p: set power rail
q: drain control buffer
s: run source
t: send traffic
v: set control period
z: change rate
x: exit
-----
```

```
GtkTerm - /dev/ttyUSB1 115200-8-N-1
strlen(stra) 3
strlen(stra + 5000) 116

-----lwIP TCP echo server -----
TCP packets sent to port 6001 will be echoed back
Start PHY autonegotiation
Waiting for PHY to complete autonegotiation.
autonegotiation complete
link speed for phy address 7: 1000
DHCP Timeout
Configuring default IP of 192.168.1.10
Board IP: 192.168.1.10
Netmask : 255.255.255.0
Gateway : 192.168.1.1
TCP echo server started @ port 7
sent 622 bytes
```

Research Project 2: University of York



References and Tools

- ▶ The most referred papers according to **Google (#cit.)**
 - ▶ Benini ([4259](#)), *Networks on Chips: A New SoC Paradigm*
 - ▶ Dally ([3866](#)), *Route Packets, Not Wires: On-Chip Interconnection Networks*
 - ▶ Kumar ([1454](#)), *A Network on Chip Architecture and Design Methodology*
 - ▶ Guerrier ([1192](#)), *A Generic Architecture for On-Chip Packet-Switched Interconnections*
- ▶ Tools
 - ▶ Simulators list
 - ▶ <https://networkonchip.wordpress.com/2011/02/22/simulators/>
 - ▶ Resources
 - ▶ <http://www.cl.cam.ac.uk/~rdm34/onChipNetBib/tools.html>

Institutions and Sponsors



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